Q.P. Code: 16CS506 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

BTECH II Year I Semester Supplementary Examinations June 2019

DIGITAL LOGIC DESIGN

(CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Subtract $(111001)_2$ from (101011) using 1's complement.	6M
	b	Convert the following numbers. i) $(AB)_{16} = (\ )_2$ ii) $(1234)_8$ iii) $(101110.01)_2$	6M

OR

2	**a**	Simplify the Boolean expressions to minimum number of literals. i) X' + XY + X Z' + XYZ' ii) (X+Y) (X+Y')	6M
	b	Write about Error correction & Detection.	6M

UNIT-II

3		Simplify the Boolean expression using K-map and implement using NAND gates F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14)	12M

OR

4	**a**	Design the circuit by Using NOR gates F= (X+Y). (X'+Y'+Z')	6M
	b	Explain NAND-NOR implementations.	6M

UNIT-III

5	**a**	Explain Design Procedure of combinational circuits.	6M
	b	Explain Full binary subtractor in detail.	6M

OR

6	**a**	Explain the functionality of a Multiplexer? With an example.	6M
	b	Explain about Priority encoder? With an example.	6M

UNIT-IV

7	**a**	Draw and explain the operation of D Flip-Flop.	6M
	b	What is state assignment? Explain with a suitable example.	6M

OR

8		Explain the working of the following with a suitable diagram i) J-K flip-flop ii) S-R flip-flop	12M

UNIT-V

9		Encode the 11-bit code 10111011101 into 15 bit information code.	12M

OR

10	**a**	Explain about Hamming Code with example.	6M
	b	Write a short notes on Programmable array Logic.	6M

*** END ***